IN THE CLAIMS:

Claims 1-14 (Cancelled).

15. (New) A wire-bond package comprising:

a substrate having a surface with a first portion and a second portion positioned relative to said first portion;

a semi-conductor chip positioned on said first portion of said surface of said substrate, said semi-conductor chip having a layer of circuitry thereon;

a first power layer and ground layer arranged in an interstitial pattern positioned on said second portion of said surface of said substrate;

a first signal ring adjacent said first power layer or said ground layer positioned on said second portion of said surface of said substrate;

an electrical interconnection between said interstitial pattern on said second portion of said surface of said substrate and said circuitry on said semi-conductor chip with two first wires each having a substantially similar first vertical height; and

an electrical interconnection between said first signal ring and said circuitry on said semi-conductor chip with a second wire having a second vertical height greater than said substantially similar first vertical height of said two first wires.

16. (New) The wire-bond package of claim 23 wherein said semi-conductor chip, said two first wires, and said second wire comprise a low profile wire-bond package of specified overall height.

17. (New) The wire-bond package of claim 23 wherein said semi-conductor chip on said first portion of said surface of said substrate comprises a chip-up configuration.

18. (New) The wire-bond package of claim 23 wherein said semi-conductor chip, on said first portion of said surface of said substrate comprises a chip-down configuration.

19. (New) The wire-bond package of claim 23 wherein said interstitial pattern on said second portion of said surface of said substrate comprises a simulated single ring configuration.

20. (New) The wire-bond package of claim 23 further comprising:

a second signal ring having a first plurality of conductive pads positioned between said first signal ring and said first power layer on said second portion of said surface of said substrate;

a second power layer arranged in a second interstitial pattern positioned between selected ones of said first plurality of conductive pads of said second signal ring and said first power layer; and

an electrical interconnection between at least one of said first plurality of said conductive pads and said second power layer with said circuitry on said semi-conductor chip using two third wires each having a substantially similar third vertical height greater than said substantially similar first vertical height of said two first wires and less than said second vertical height of said second wire.

21. (New) The wire-bond package of claim 28 wherein said semi-conductor chip, said two first wires, said second wire and said two third wires comprise a low-profile wire-bond package of specified overall height.